Electroless metal deposition for IC and TSV applications.

James F. Rohan, Declan Casey, Monika Zygowska, Michael Moore, Brian Shanahan
Electrochemical Materials & Energy,
Tyndall National Institute,
University College Cork, Ireland
james.rohan@tyndall.ie

***Abstract*—Ultrathin film electroless deposition of Cu and Ni is shown for IC and TSV barrier layer / interconnect applications as an alternative to vacuum based deposition techniques. Cu films of approximately 20 nm were achieved while coherent electroless Ni can be deposited to single digit nm levels. The use of self-assembled monolayers facilitates electroless deposition in high aspect ratio structures. This activation process in combination with ultrathin film barrier/seed layer deposition by electroless processing enables scaling for both IC and TSV interconnect applications.**

Keywords—electroless; metal; deposition; thin film; interconnect; barrier layers; TSV

I. INTRODUCTION

Electrochemical deposition for on-chip interconnect has over the past two decades inspired many aspects of nanoscale electrochemical processing. The detailed analysis of the electrolytic route has resulted in a continuous scaling that has matched the requirements of the International Technology Roadmap for Semiconductors (ITRS). Electroless deposition is an electrochemical process to deposit thin films on substrates with the aid of a chemical reducing agent and without an external power supply. It is a potential batch process that unless specifically modified produces conformal films. Electroless processing has already shown significant potential for IC interconnect applications in self-aligned capping layer deposition on Cu [1].

In damascene processing overdeposited Cu is removed by chemical mechanical polishing (CMP). The CMP produced top Cu surface is the fast Cu diffusion path which needs to be tightly capped. A nonconductive barrier layer is generally applied as the cap layer (e.g. silicon nitride, silicon carbide, nitride silicon carbide, etc.) to cover the top surface of the Cu line. However, there are some issues with using dielectric caps to passivate Cu. As devices become smaller, the current density through the interconnect increases leading to the requirement for better electromigration resistance and higher current capability. Improved Cu electromigration resistance has been reported for thin conductive surface capping layers of self-aligned electrolessly deposited Co alloys CoWP or CoSnP [2, 3].

The active Cu interconnect material can also be deposited using electroless deposition and plating bath additives that operate in much the same way as those used in electrolytic baths. Extension of this processing to the larger dimension TSV is possible while also providing potential ITRS roadmap solutions for the high aspect ratio barrier, seed layer and active interconnect deposition.

Electroless plating baths are complex solutions typically involving multistep oxidation [4, 5] and metal reduction. Common to both electrolytic and electroless deposition for future Cu based IC or TSV interconnect is the need to utilise additives to enhance the deposition characteristics. The additives typically employed in damascene plating are based on the interaction between PEG type materials and an accelerator. Controlled electroless processing for barrier and seed layers that are thin and conformal is required. The results presented here indicate the limits of electroless processing for ultrathin film deposition of coherent films.

II. EXPERIMENTAL

All chemicals used were purchased from Sigma Aldrich and used as received. Deionised water of resistivity 18 MΩ cm was used to prepare the solutions. The electroless solutions were prepared in glass beakers and the temperature maintained using an Ikamag RCT stirring hotplate with an Ikatron ETS-D4 electronic thermometer and IKA H 60 temperature probe. All experiments were performed with magnetic stirring at 100 rpm. Electroless bath pH was adjusted using ammonium hydroxide.

Electrochemical analysis was performed under PC control with a CHI 660C potentiostat from CH Instruments. An in-house Teflon cell holder with contacts to the Au working electrode microdisc array, a Pt counter electrode and a Pt pseudo reference on Si was utilised for microelectrode array analysis.

The deposited material selectivity and morphology was analysed using an FEI Quanta FEG 650 field-emission scanning electron microscope. Elemental analysis was performed using an Oxford Instruments EDX (X-MAX 20 large area Si diffused detector) HRTEM imaging was performed on a JEOL 2100

High Resolution (Scanning) Transmission Electron Microscope. A FEI Helios NanoLab 600 Dual Beam FIB with in-situ lift-off for cross-sectional TEM sample preparation was used. Initial deposit thickness and uniformity was determined using a Tencor Alpha-Step 200 surface profilometer and correlated with data measurements recorded on the HRSEM/TEM.

III. RESULTS AND DISCUSSION

One aspect in the optimisation of electroless deposition is an assessment of the bath constituents and their role in the deposition process. Previous analysis has investigated the DMAB oxidation mechanism in strongly alkaline solutions [4, 5]. Electroless deposition baths typically operate at less alkaline pH and this has been analysed using microelectrode arrays fabricated on Si. The Au microdisc electrodes of 20 μm in diameter and 500 μm separation gave the following comparison for DMAB oxidation in 1 M NaOH and the less alkaline 0.01M NaOH in Fig. 1.

It can be seen that the oxidation current is decreased which translates into a less reactive reducing agent at lower pH values. Based on experimental observations the oxidation reaction even at the lower pH is sufficient to achieve quite high rates of electroless materials deposition (~ 10 μm/hr) by comparison with alternative deposition techniques such as atomic layer deposition (ALD). A less reactive reducing agent for more controlled deposition is desirable for nanoscale deposition particularly on 3D substrates.

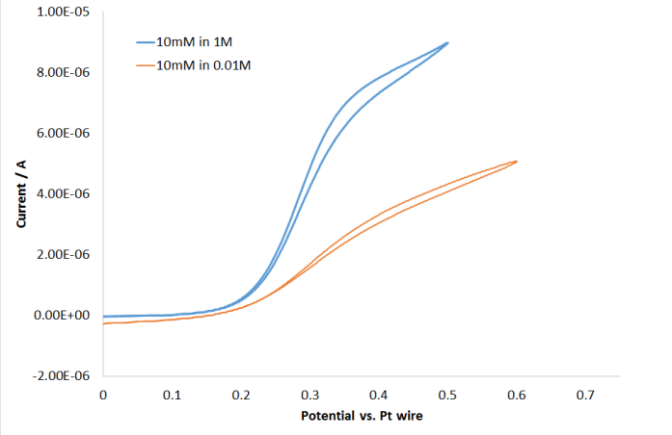

Fig. 1. DMAB oxidation at a Au microelectrode array at 100 mV/s. The concentration of DMAB in NaOH is shown on the chart.

A comparison of the morphology of thin film electroless Cu and ALD deposited Cu (Fig. 2 and 3) shows that the same issue of island-like growth places a limit of approximately 20 nm on the thickness of coherent Cu films.

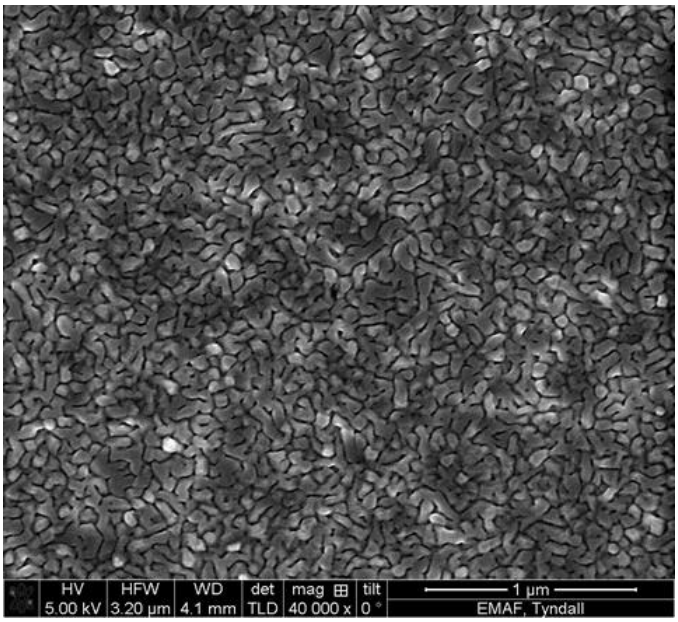

Fig. 2. SEM analyss of thin film electroless Cu showing island-like growth.

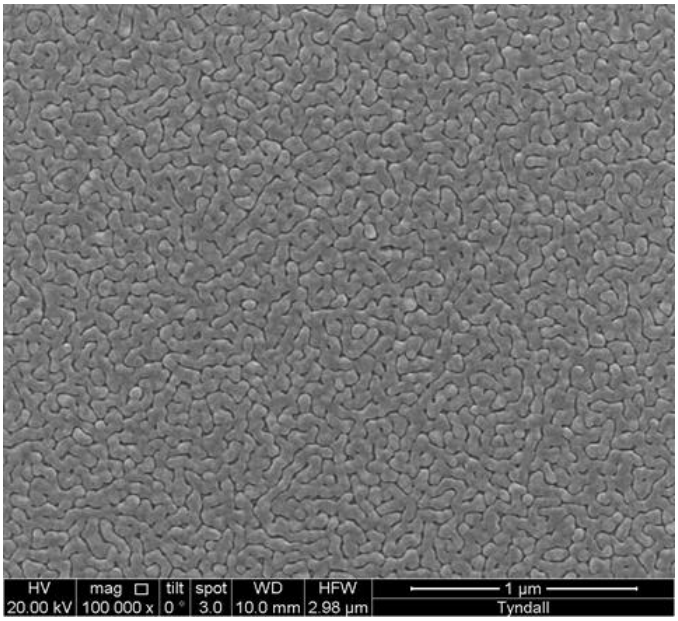

Fig. 3. SEM analyss of thin film ALD Cu showing island-like growth.

Silicon substrates with a 2 nm native oxide coverage were treated with 3-Aminopropyl) triethoxysilane (APTES) self-assembled monolayer to facilitate palladium activation. Cross sectional HRTEM analysis of first the Pd activated substrate, Fig. 4, shows that at the level required to facilitate Cu deposition Pd could not be detected on the substrate. The Cu deposit formed on the Pd activated APTES is shown in the HRTEM of Fig. 5. This is the minimum thickness achieved for electroless Cu deposition on Pd activated substrates and correlates well with observations for coherent film ALD Cu deposition.

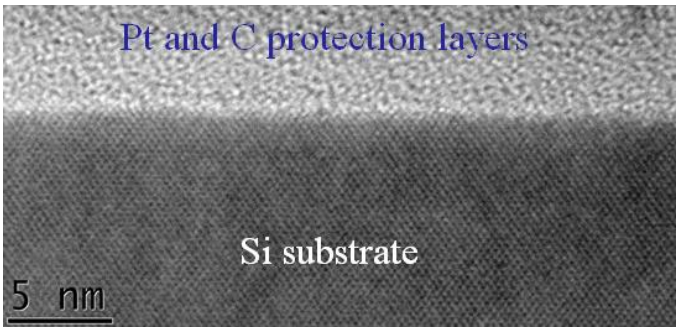

Fig. 4. HRTEM analyss of native oxide on silicon following activation with Pd on APTES self assembled monolayer. Pd is not detected at the interface.

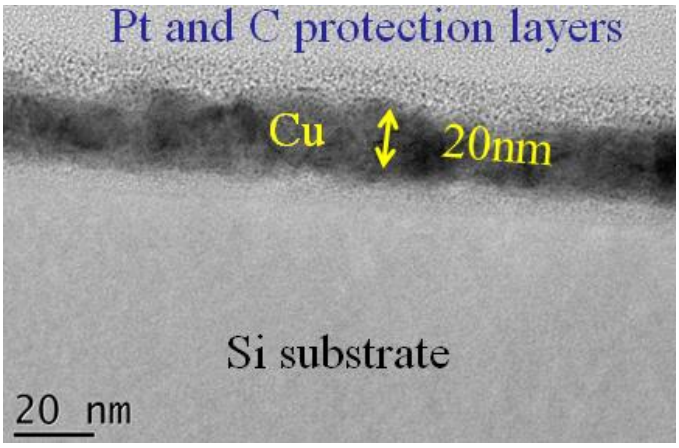

Fig. 5. HRTEM analyss of thin film electroless Cu on native oxide on silicon following activation with Pd on APTES self assembled monolayer.

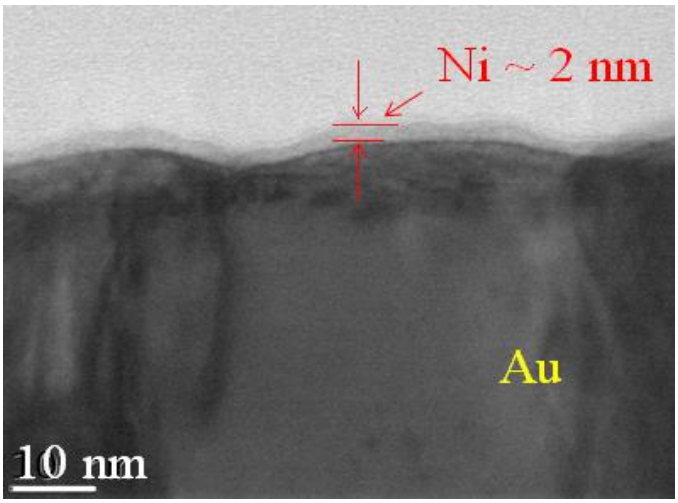

Fig. 6. HRTEM analyss of thin film electroless Ni on patterned Au pads over Cr on Si. The electroless Ni layer thickness is on average 2 nm.

Optimisation of electroless Ni plating solutions enabled ultrathin film deposition on patterned Au pads on Si. HRTEM indicated that films down to 2-3 nm could be achieved with Ni. This is appropriate as a barrier layer thickness for IC level Cu interconnect. It also indicates that there is significant process modification that can be employed to achieve metallisation of high aspect ratio TSV structures which are still in the micron range. Ultrathin film Ni barriers for subsequent electroless Cu TSV fill are therefore viable as an alternative metallisation route for future scaling of electronic devices.

IV. CONCLUSIONS

Electroless Cu and Ni ultrathin film deposition on planar and patterned substrates has been achieved. TEM analysis of blanket and selective deposition shows ultrathin films extending down to 2 nm. Pd activated self-assembled monolayers have enabled direct ultrathin electroless metallization of dielectric materials.

ACKNOWLEDGMENT

The ALD Cu image was supplied by Martyn Pemble and Dirk Hagen at Tyndall. The authors thank Michael Schmidt for TEM analysis. This research was part resourced by the iTech project within CCAN - the Collaborative Centre for Applied Nanotechnology (www.ccan.ie), supported by Enterprise Ireland & IDA Ireland (grant no. CC/2012/06a); the Science Foundation Ireland Technology Development innovation award (grant no. 12/TIDA/I2355); the Enterprise Ireland Commercialisation Fund project Intecell (grant no. CF/2012/2341) co-funded by Enterprise Ireland and the European Regional Development Fund (ERDF) under the National Strategic Reference Framework (NSRF) 2014-2020.

REFERENCES

[1] J.F. Rohan and D. Thompson, "Frontiers of Cu Electrodeposition and Electroless Plating for on-chip Interconnects" in Copper Electrodeposition for Nanofabrication of Electronic *Devices*. Vol 171. (2014) K. Kondo, R.N. Akolkar; D.P. Barkey and M. Yokoi, Eds. Springer (US) 2014. pp. 99-113

[2] E. Liniger, J. Rubino, C. Sambucetti, *Microelectron. Eng.*, **70,** 406 (2003).

[3] J. Gambino, J. Wynne, J. Gill, S. Mongeon, D. Meatyard, B. Lee, H. Bamnolker, L. Hall, N. Li, M. Hernandez, P. Little, M. Hamed, I. Ivanov, C. Gan, *Microelectron. Eng.*, **83,** 2059 (2006).

[4] L.C. Nagle, J.F. Rohan, *Electrochem. Solid-St.*, 8 (2005) C77;

[5] L.C. Nagle, J.F. Rohan, *J. Electrochem. Soc.*, 153 (2006) C773